

This listing of claims will replace all prior versions, and listings, of claims in the application:

**The Status of the Claims**

1. (Original) A method for fabricating a nonvolatile memory device comprising:

forming an isolation layer and a non-active region in a semiconductor substrate;

forming an oxide layer and a polysilicon layer on the substrate;

forming a sacrificial layer on the polysilicon layer;

patterning the sacrificial layer to form polymer layers on sidewalls of the sacrificial layer, the polymer layers being generated from the etching of the sacrificial layer; and

forming a floating gate and a tunnel oxide using the sacrificial layer and the polymer layers as an etching mask.

2. (Original) A method as defined in claim 1, further comprising:

removing the polymer layers and the sacrificial layer; and

forming an insulating layer and a polysilicon layer over the substrate, the floating gate, and the tunnel oxide.

3. (Original) A method as defined in claim 1, wherein the sacrificial layer is formed of one selected from the group consisting of TEOS (tetraethyl orthosilicate) oxides and nitride.

4. (Currently Amended) A method as defined in claim 1, wherein a space between a two adjacent polymer layers is between ~~300 and 1200~~ 300 Å and 1200 Å.

5. (Currently Cancelled)

6. (Currently Amended) A method for fabricating a nonvolatile memory device comprising:  
forming a first floating gate; and  
forming a second floating gate adjacent the first floating gate, the first and second floating gates being separated by less than a lithographic minimum feature size.[]]